REMARKS

Claims 1-2 and 4-6 are pending in this application, of which claims 4-6 have been amended. No new claims have been added.

Claims 5-6 stand rejected under 35 USC §112, second paragraph, as indefinite.

Accordingly, claims 5-6 have been amended to correct some of the noted instances of indefiniteness. It should be noted that page 5, line 22 of the specification clearly shows that fc is a comparison signal, as recited in claim 1, and the second embodiment shown in Fig. 6 shows switch circuit 6 for switching the comparison signal inputted to the phase comparator 1.

Thus, the 35 USC §112, second paragraph, rejection should be withdrawn.

Figs. 7-9 have been labeled as "Prior Art", as required by the Examiner.

Before turning to the cited reference, a brief review of the claimed invention is in order.

The present invention is a PLL circuit which compensates for stoppage of PLL operations when the voltage control oscillator 3 oscillates abnormally and the operation of the frequency divided 4 stops such that the operation returns to the normal state. In order to realize this object, the present invention comprises an operation stoppage detecting means for detecting that PLL operation has stopped, said detection being effected on the basis of an output signal from the voltage control oscillator or the frequency divider; and a control means for controlling the voltage control oscillator such that an oscillation frequency of the voltage control oscillator is low.

Claims 1, 2 and 4-6 stand rejected under 35 USC §103(a) as unpatentable over JP 10-107627 to Masatoshi (hereinafter "**Masatoshi**").

Applicants respectfully traverse this rejection.

Masatoshi discloses a PLL circuit in which a control signal "A", which is outputted from a low-pass filter 16, is inputted to a control circuit 20. The circuit 20 detects a voltage level of the control signal "A" and detects whether or not a PLL circuit 10 is in a deadlock state. If the circuit 10 is in a deadlock state, the circuit 20 outputs a detection signal which is in an active state to recover it into a normal locked state. That is, the voltage level of a control signal detects that the circuit 10 reaches a certain voltage level where there is a possibility that it falls into a deadlock state and further, that it is in a deadlock state, and reduces the voltage level of the control signal "A".

Thus, **Masatoshi** restores the abnormal operation of the entire circuit to the normal state though different in its means of doing so from the present invention; that is, when the VCO ceases to oscillate a comparison signal fc and the control voltage Vc issued from the loop filter reaches or exceeds a predetermined level, a detection signal is fed to the charge pump circuit to lower the control voltage such that the oscillation is restored.

In this respect, the present invention claims the detection being effected on the basis of an output signal from the voltage control oscillator or the frequency divider. In **Masatoshi**, on the other hand, the detection signal is not issued unless the VCO ceases to oscillate and then, the control voltage of VCO reaches or exceeds a predetermined level. Such roundabout procedure of monitoring of the control voltage causes delay or unevenness in detection unlike the direct way as claimed.

In this way, the present invention has an improved and faster way of detecting the

malfunction of the VCO than can be obtained by **Masatoshi**.

In summary, in **Masatoshi**, the control signal A is outputted from the LPF. This is in contrast to the present invention, in which the detection is "effected on the basis of an output signal from said voltage control oscillator or frequency divider", as recited in claim 1 of the instant application.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-2 and 4-6, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures:
Replacement Sheets of Drawing (Figs. 7-9)

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